Dielectrics at the III-V logic starting gate

The IEEE's International Electron Devices Meetings of the past few years have seen an increasing development of III-V semiconductor channels for use as silicon logic enhancers. Last December, the focus for IEDM 2009 shifted from the demonstration of the benefits of high mobility and integration with silicon substrates to developing the gate stack. Mike Cooke reports.

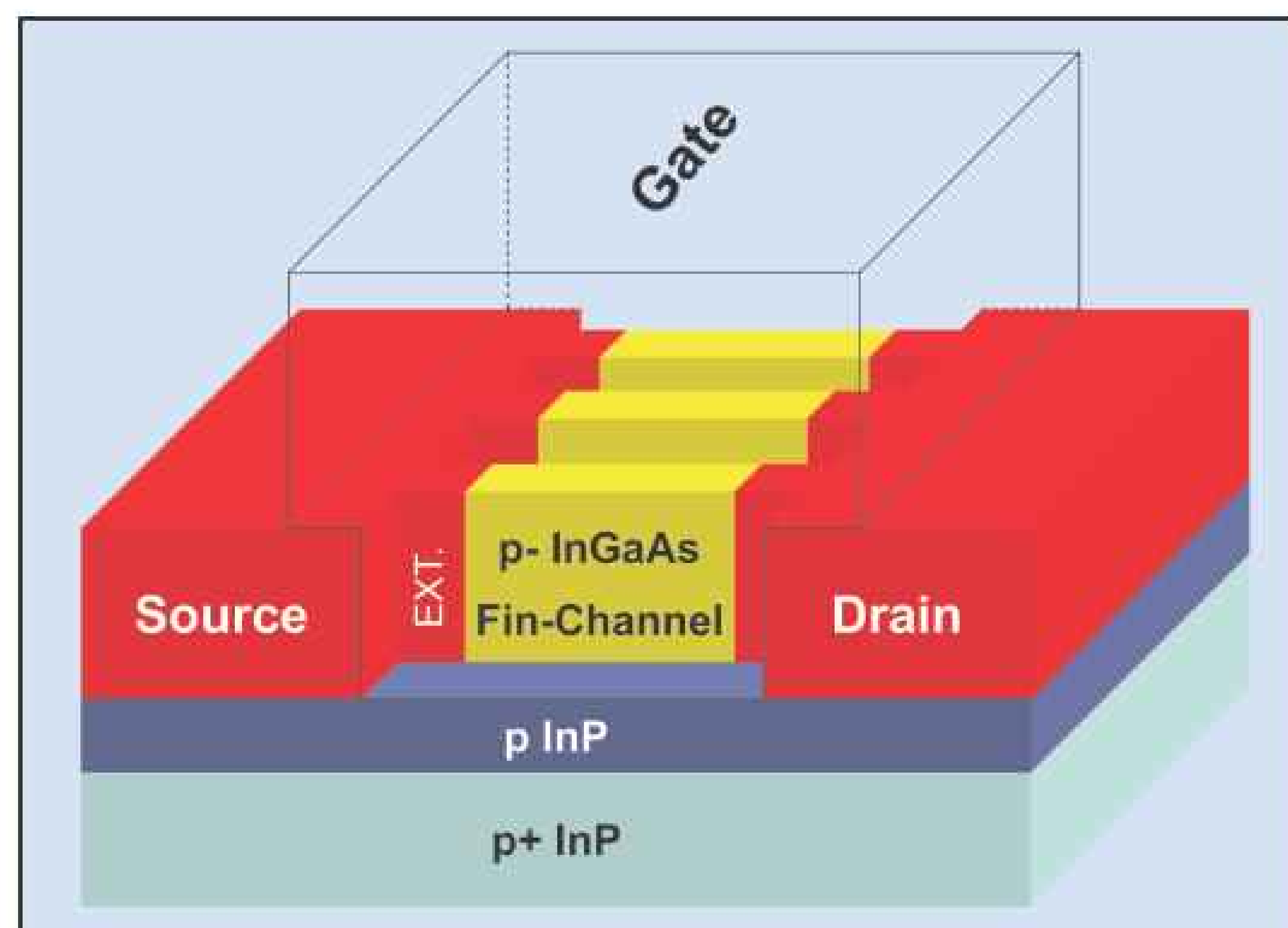

Figure 1. Schematic of Purdue's InGaAs FinFET.

A wide range of electron device developments (that also shifts with the years) gets to be reported and discussed each December at the IEEE's International Electron Devices Meeting. About half of the work tends to be mainstream silicon CMOS with potential application in the next few years. Some sessions look into the far future (2020s and beyond), for which the present interest seems to be mainly focused on carbon-based devices — nanotubes and graphene.

Here we will focus on the medium-term issue of gate dielectrics for use with III-V logic devices designed to solve (for a time) many of the problems raised by the continuous shrinking of CMOS devices on silicon according to the schedule set out in the International Technology Roadmap for Semiconductors (ITRS). The development of nitride and silicon carbide power transistors will be the subject of a future article.

The mainstream logic industry (e.g. Intel) is looking to III-V materials such as indium gallium arsenide (InGaAs) and indium antimonide (InSb) to create channels with higher drive currents on the basis of higher charge-carrier mobility. The complementary metal-oxide-semiconductor/silicon (CMOS) circuits used in the logic industry need both n-type nMOS and p-type pMOS field-effect transistors (FETs), where inversion layer channels have current carriers that have negative ('electron') and positive ('hole') charge, respectively.

While hole mobility in silicon is reduced by a factor of three compared with that of electrons, the situation is often much worse with the III-V contenders for CMOS enhancement (typically, a factor of 20–100 lower). It seems likely that germanium channels will be used for high hole mobility, although some recent modeling work — involving Stanford University, Intel and the US Naval Research Lab [1] — suggests that a strained indium gallium antimonide (InGaSb) combination could achieve better hole mobility. Experiments with $In_{0.41}Ga_{0.59}Sb$/GaSb resulted in the highest reported hole mobilities, at 3x that achieved with uniaxially strained silicon.

The higher electron mobility of bulk InGaAs (more than 8000cm^2/V-s) compared with bulk silicon (~1500cm^2/V-s) leads to larger currents in the on-state. However, off-state performance needs to be much improved to meet the requirements of the International Technology Roadmap for Semiconductors (ITRS). Off-state short-channel effects (SCEs) in InGaAs kick in much faster due to its narrower bandgap and higher dielectric constant (k) compared with silicon.

FinFETs

Wrap-around gate structures, such as those around the fin channels in FinFETs, provide better electrostatic control of the off-state. This requires highly challenging etch processes with low surface damage

and a good interface with high-k gate dielectrics. Dry (plasma) etch of III-V materials such as InGaAs can be particularly tricky.

Purdue University is claiming the first 'well behaved' inversion-mode (i.e. normally-off) indium gallium arsenide (InGaAs) FinFET (Figure 1) with gate lengths down to 100nm [2]. The gate dielectric comprised aluminum oxide (Al_2O_3), deposited using atomic layer deposition (ALD) techniques. The fin height was 40nm.

The researchers report much better control of SCEs, compared with normal planar InGaAs MOSFETs, resulting in improved sub-threshold slope (SS, 34% better with 100nm gate length, compared with planar devices), drain-induced barrier lowering (DIBL, reduced from 480mV/V to 180mV/V) and threshold voltage (V_T) roll-off (about 30% that of a planar device), along with less degradation of these properties at raised temperature (up to 360K).

In related work, Purdue has developed a new hydrogen bromide (HBr) pre-treatment, along with retrograde channel structuring and halo-implantation, to improve the InGaAs/high-k dielectric interface for planar MOSFETs [3]. Both the FinFET and the planar MOSFET work were led by Purdue doctoral student Yanqing Wu.

Although the ultimate aim would be to create InGaAs FinFETs on silicon substrates up to 300mm diameter and beyond, the Purdue researchers used a 2-inch indium phosphide substrate for the 'proof-of concept' device (Figure 1). The device layers were grown using molecular beam epitaxy (MBE). A heavily doped InP layer was grown beneath the $In_{0.53}Ga_{0.47}As$ channel to reduce punch-through of current in the off-state and current leakage through the substrate. One negative effect of the high doping was worse junction leakage due to the non-optimized contacts that were used.

An Al_2O_3 dielectric 'encapsulation layer' was then grown to a thickness of 10nm using an ASM F-120 reactor. The source and drain regions were created using selective ion implantation of Si through the dielectric into the InGaAs followed by rapid thermal annealing (RTA) to activate the Si doping.

The fin structures were created using a combination of wet and dry etch techniques, resulting in damage-free sidewalls. The dry etch used a boron trichloride (BCl_3)/argon (Ar) plasma. An electron-beam lithography resist (ZEP-520A) was used as a mask for the etch process. The surface layer damage from the dry etch was removed using a 3 second dip in a dilute sulfuric acid/hydrogen peroxide H_2SO_4:H_2O_2:H_2O solution. The researchers believe a more sophisticated process is needed to create more vertical side-walls (Figure 2).

The Al_2O_3 encapsulation was removed with a buffered-oxide etch (BOE) solution. The Al_2O_3 dielectric was then re-grown as a 5nm gate dielectric film after an ammonium sulfide ($(NH_4)_2S$) surface preparation.

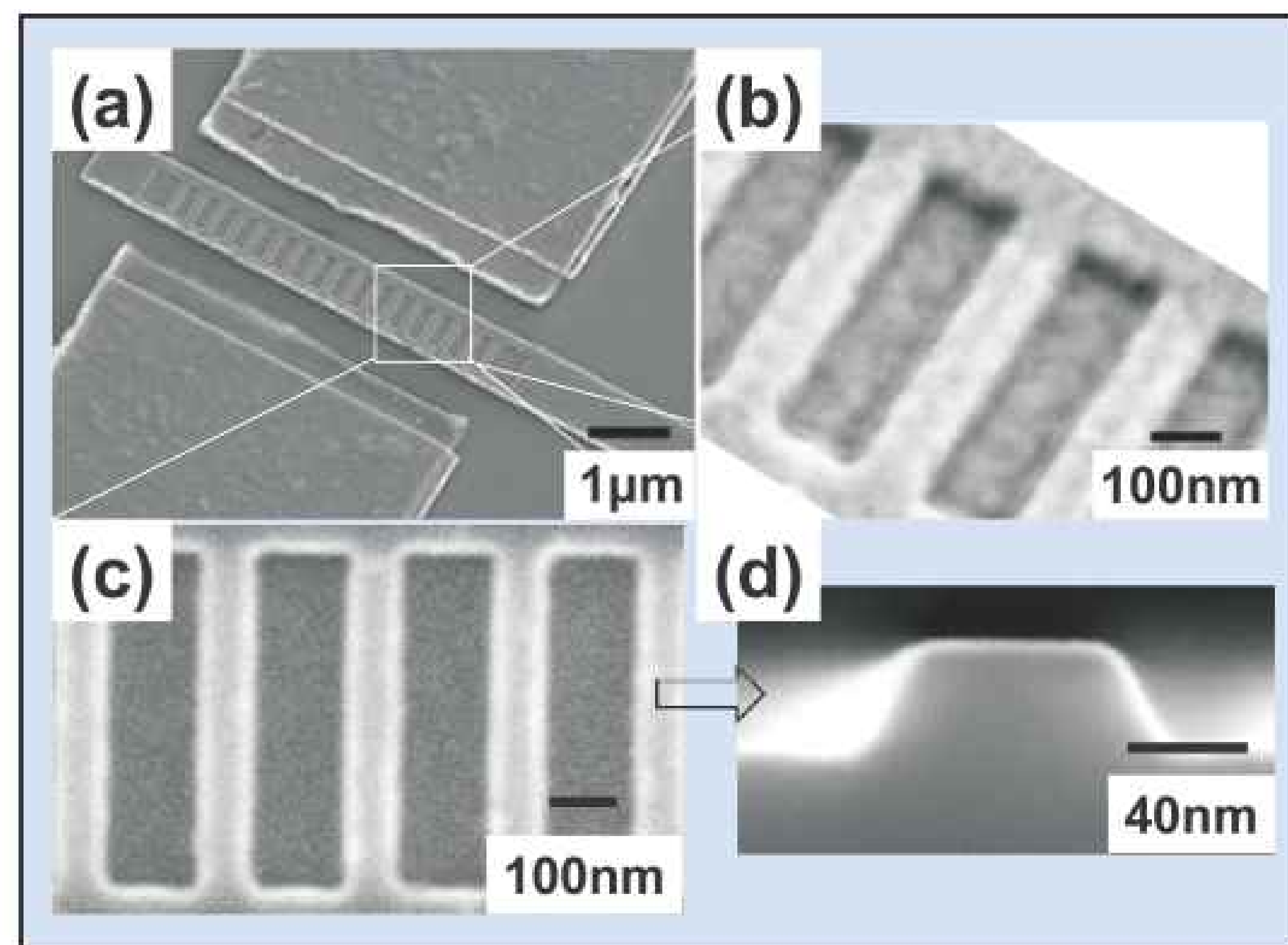

Figure 2. Tilted SEM image of Purdue's FinFET device. (b) Zoomed-in image of channel region covered with gate dielectric and metal. (c) SEM image of the fin structure after dry etching. (d) Cross sectional SEM image of fin after dry etching.

Electron-beam evaporation and lift-off was used to form the source/drain contacts using AuGe/Ni/Au layers. The gate was Ni/Au, created similarly.

The improved sub-threshold slope (SS) for the device is taken as an indicator of the 'damage-free' nature of the etch process of the fin. Normally, planar device interface trap densities can be estimated from the variation of SS values with temperature. Since the FinFET cannot have better surface quality than the planar device, the better overall SCE behavior must impact the SS performance. However, the very good SS values obtained indicate high-quality interfaces, enabling the researchers to declare that the dry/wet etch process is 'damage free'. By making suitable extrapolations, the Purdue team estimates an upper limit on the average interface trap density (D_{it}) of $1.7x10^{12}/cm^2$-eV.

The Purdue researchers also claim to be the first to grow hafnium dioxide (HfO_2) dielectric on fin-structures, in work yet to be published. HfO_2 dielectric is among the leading contenders for use as high-k dielectric on traditional CMOS transistors. Companies such as Intel and IBM have both proposed its use.

Composite stacks

The focus for Intel's latest reported work on InGaAs channels has been the gate contact, and particularly reducing leakage through using high-k dielectric insulation, rather than a Schottky contact [4].

A composite gate stack on $In_{0.7}Ga_{0.3}As$ was made (Figure 3) using 4nm of tantalum silicon oxide ($TaSiO_x$) and 2nm of indium phosphide. The dielectric was applied using atomic layer deposition (ALD) on the upper barrier rather than directly on the well to maintain the channel mobility (measured at

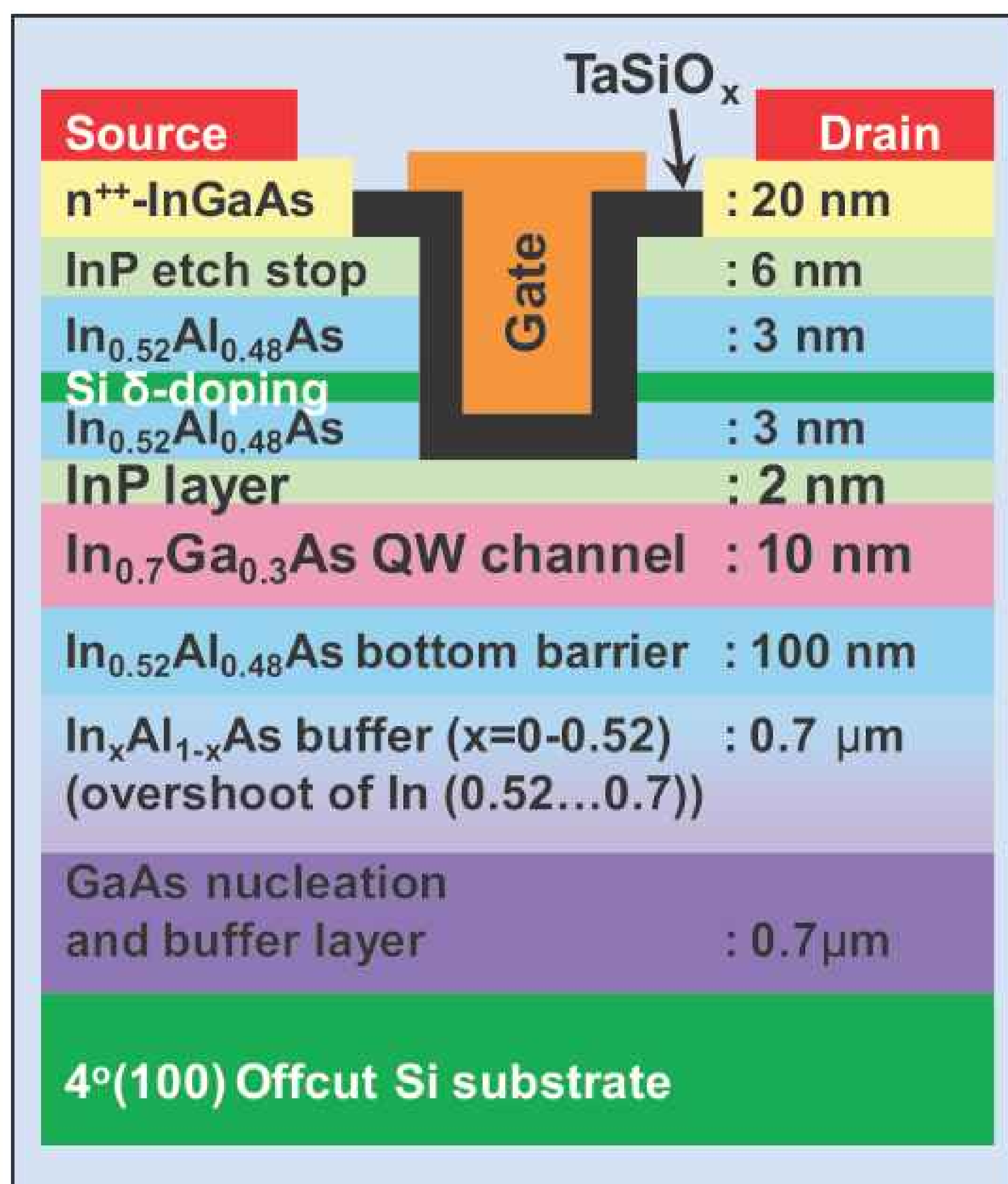

Figure 3. Schematic of $In_{0.7}Ga_{0.3}As$ QWFET on silicon with 2nm InP upper barrier layer and a 4nm $TaSiO_x$ high-k gate dielectric, forming composite $TaSiO_x$-InP gate stack. Reprinted by permission of Intel Corp, Copyright Intel Corp.

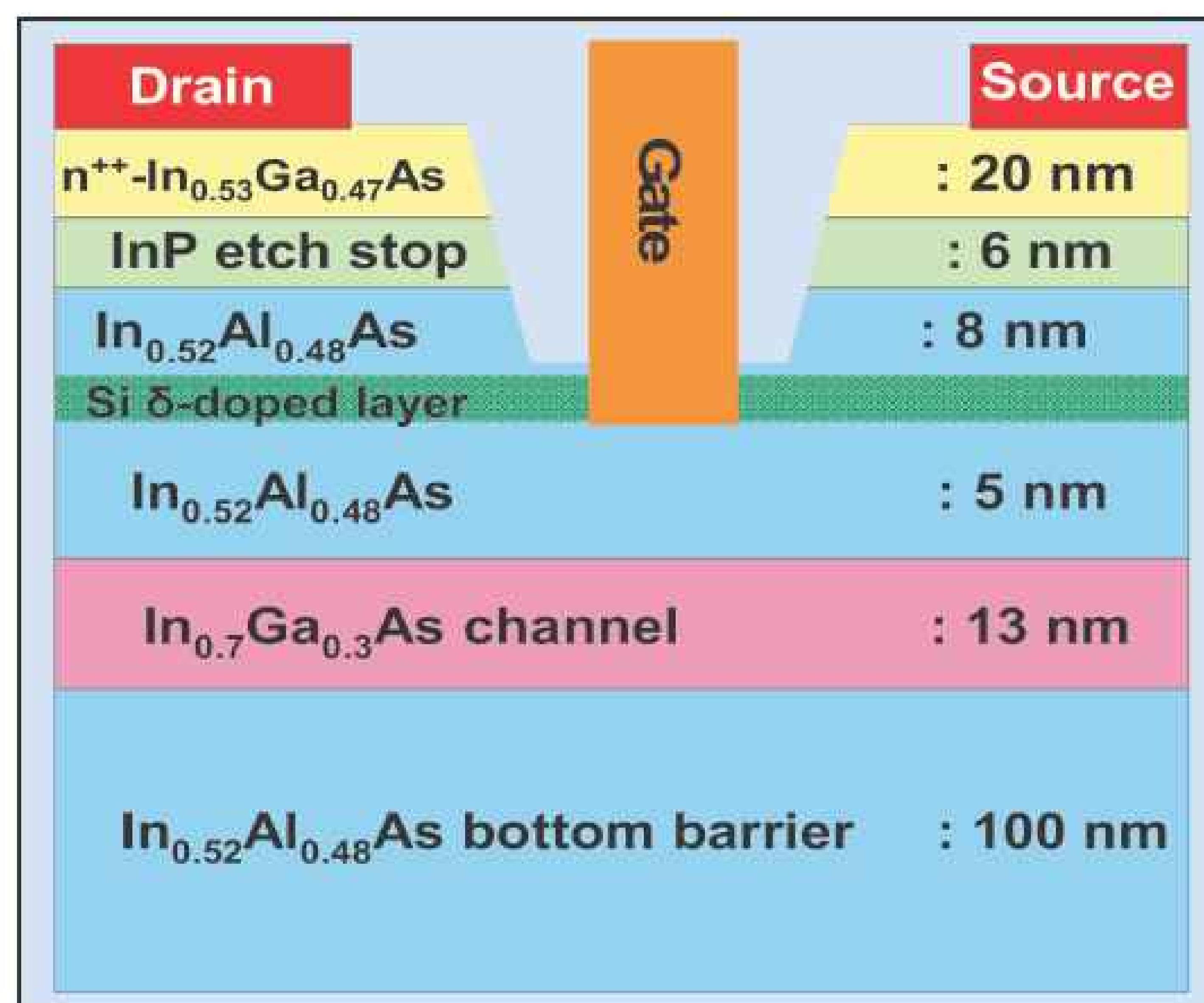

Figure 4. Schottky-gate $In_{0.7}Ga_{0.3}As$ QWFET with remote delta doping (Si doping ~ $8x10^{12}/cm^2$) and Pt gate electrode. Reprinted by permission of Intel Corp, Copyright Intel Corp.

$10,000cm^2$/V-s at 300K with no parallel conduction). The process steps to produce the stack consisted of cleaning, and then depositing a thin transition layer and then the dielectric.

A quantum well channel was used in a field-effect transistor (QWFET) format with a physical gate length of 75nm. Capacitance–voltage measurements give an electrical oxide thickness (t_{OXE})of 22Å. Control devices with a Schottky gate managed a t_{OXE} of only 33Å. The dielectric reduced the gate leakage by a factor of more than a thousand.

The drive current was 0.49mA/µm and the peak transconductance was 1750µS/µm at a V_{DS} of 0.5V, which are the highest reported values for III-V QWFETs with high-k gate dielectric, according to the researchers. Comparing the devices with strained silicon MOSFETs, one finds a 3.5x effective electron velocity.

Intel is also continuing to work on $In_{0.7}Ga_{0.3}As$ 80nm QWFET devices with a Schottky gate contact [5], comparing logic performance against that of advanced strained Si 40nm MOSFETs with supply voltages of between 0.5 and 1.0V, at constant I_{off} (Figure 4). The effective electron velocity in the QWFET channel is 4.6–3.3x that in a comparison strained silicon device. This enables a 65% drive current gain at an operating voltage (V_{CC}) of 0.5V and 20% at 1.0V, despite the 2.5x lower charge density in the QWFET channel. Despite the longer gate length, the QWFET shows improved gate delay properties over the strained Si MOSFET. Temperature dependence studies indicate that the charge carriers in the QWFET suffer from phonon surface roughness scattering, so the device is not in the ballistic regime. This means that the mean free path is less than the distance of travel in the QWFET device.

The Intel work was carried out jointly with researchers from epiwafer foundry IQE in Pennsylvania. The Intel contribution was based in Oregon. IQE's facility produced the semiconductor layer structures as InGaAs QWFET epiwafers grown on Si substrates using molecular beam epitaxy (MBE). Intel then used the blanket epiwafers for their transistor design and fabrication.

IQE also provided material for the research by Purdue University [2, 3], and for work by Cornell and Penn State universities [6]. The Cornell/Penn State research included an IQE representative in the author list. This research involved $In_{0.53}Ga_{0.47}As$ vertical inter-band tunnel field-effect transistors (TFETs) with a 100nm channel length. A high-k/metal gate was used, aiming for ultra-low-power devices. The TFET device had an 'on-current' of 20µA/µm at 0.75V, and a large on–off current ratio of 104, given the channel length of 100nm. A six-transistor (6T) TFET SRAM cell with virtual ground assist was demonstrated.

Common process step

The IMEC semiconductor research center based in Belgium has been studying a common gate stack solution (Figure 5) for InGaAs/Ge structures [7]. The researchers see integrated high-mobility channels with high-k dielectric gate stacks as "a leading

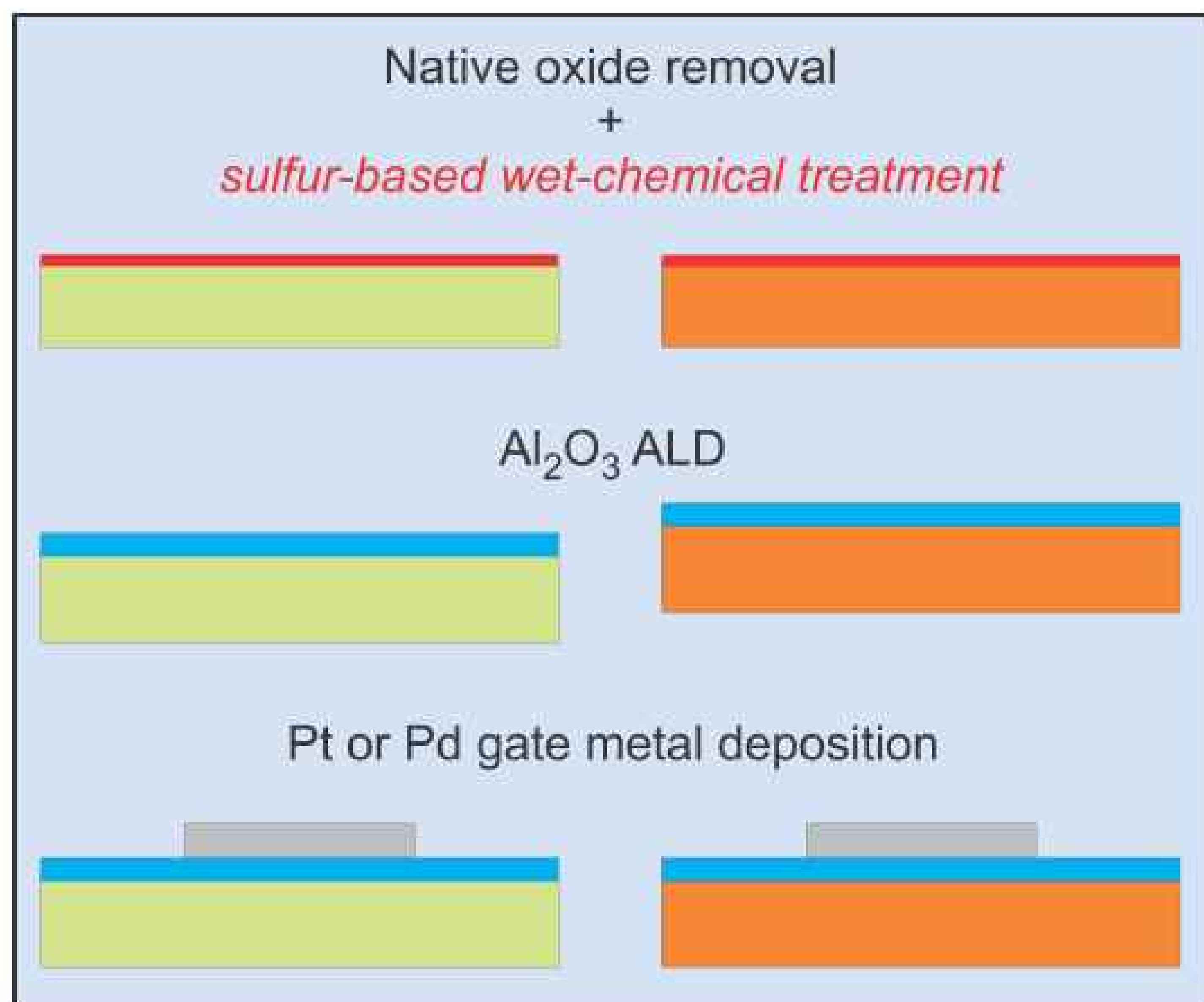

Figure 5. Common Gate Stack (CGS) process for InGaAs/Ge MOS devices developed by IMEC.

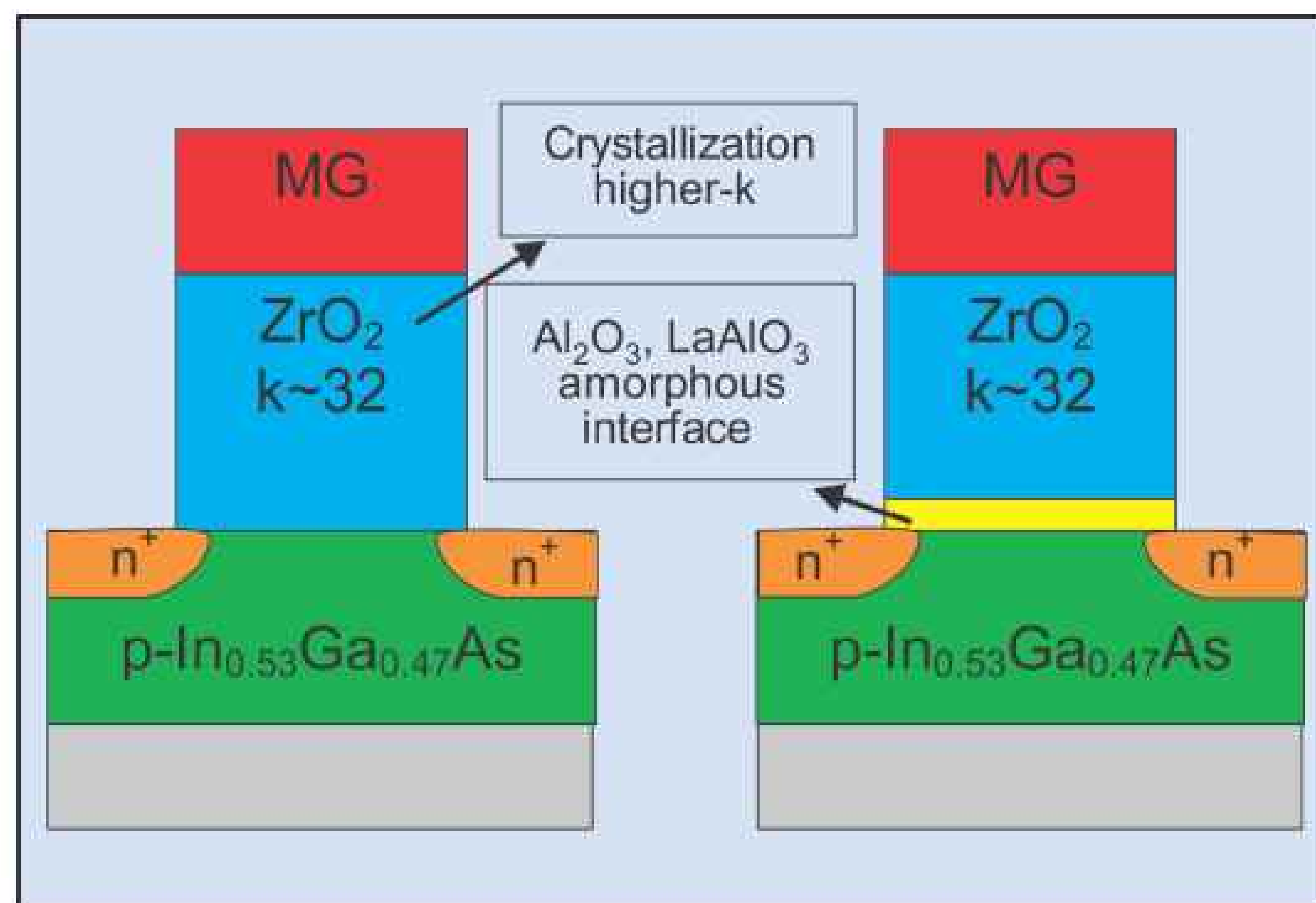

Figure 6. 'Cartoon' of SEMATECH nMOSFETs using zirconia dielectric. Various thicknesses (0.3 to 2nm) of ALD Al_2O_3 or $LaAlO_3$ interlayer were deposited prior to ZrO_2 deposition. TiN/TaN was used as the metal gate (MG).

candidate for the next-generation technology on and beyond the 16nm node". The ITRS has renounced the idea of a simple 'node' for describing technology pacing in its latest edition (2009). The physical gate length for microprocessors is expected to reach 15.3nm in 2016; and, for the half-pitch for metal lines (the traditional ITRS 'node' measurement), 15.0nm in 2018.

The aim of IMEC's research is to find a route to providing common gate stacks for InGaAs n-MOSFETs and Ge p-MOSFETs to combine into CMOS circuitry. The team's approach is to use a sulfur-based wet chemical pre-treatment and then use atomic layer deposition (ALD) of aluminum oxide (Al_2O_3) to give the gate dielectric. The researchers want to find a feasible solution for both InGaAs/Ge CMOS process integration and progressive equivalent oxide thickness (EOT) scaling.

Although the ultimate aim must be to deposit gate dielectric on InGaAs and Ge channels on one substrate, the IMEC experiments used separate InGaAs and Ge substrates on which to create MOS capacitors and transistors. The surface preparation consisted of cleaning and oxide removal followed by wet chemical treatment with ammonium sulfide ($(NH_4)_2S$) solution.

The Al_2O_3 was deposited at 300ºC with a thickness of 8nm on Ge and 10nm on InGaAs. A post-deposition anneal in forming gas (N_2/H_2) was carried out at 400ºC. The capacitor/gate electrodes consisted of 'high-work-function metal'.

The interface traps in the two systems were investigated using capacitance–voltage (CV) and conductance–voltage (GV) measurements. Near the Ge valence band edge, the interface trap density (D_{it}) was relatively low at $3x10^{11}$/eV-cm^2, increasing towards the conduction band edge to a high value of more than $1x10^{13}$/eV-cm^2. For InGaAs, a relatively low D_{it} of $1x10^{12}$/eV-cm^2 was found near the conduction band, increasing to more than $2x10^{13}$/eV-cm^2 near the valence band.

These are appropriate characteristics for creating MOSFETs on the two materials. MOSFETs with 10µm gates were constructed that had peak hole (Ge) and electron (InGaAs) mobilities of 400cm^2/eV-s and 1300cm^2/eV-s, respectively. These values are comparable to separate mobility records for Ge and InGaAs channel technologies of 445cm^2/eV-s and 1600cm^2/eV-s, respectively.

Table1. Comparison of ZrO_2, 1nm Al_2O_3/ZrO_2, and 1nm $LaAlO_3/ZrO_2$ on $In_{0.53}Ga_{0.47}As$.

Interlayer		ZrO_2	Al_2O_3	$LaAlO_3$
Interface state trap density, D_{it} @ E_v = +0.42eV	$10^{12}eV^{-1}cm^{-2}$	2.03	–0.7	0.7
Interface fixed charge density, Q_f	$10^{12}cm^{-2}$	7.8	2.4	–
Border trap density, Q_{br}	$10^{19}cm^{-3}$	7.5	2.6	–
Hysteresis/ capacitance equivalent thickness (CET)	MV/cm	2.53	2.17	1.27
Interface trap charge density, Q_{it}	$10^{12}cm^{-2}$	6.9	4.6	–
Dielectric constant, k		–32	–7	–12
Threshold voltage, V_t	V	–0.12	0.07	–
Transconductance (Gm) x CET	µS-nm	3359	5883	–

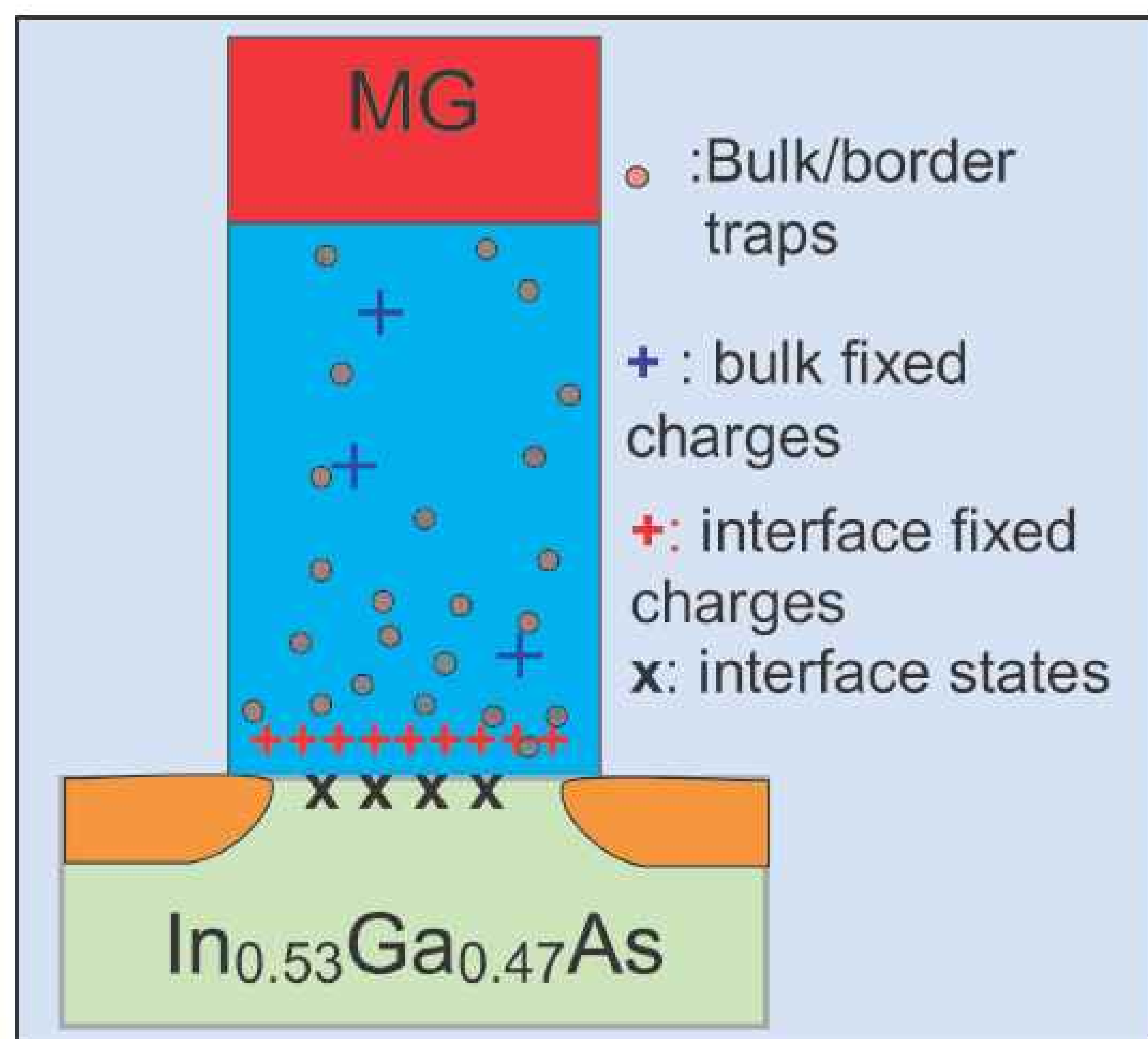

Figure 7. Schematic of charge/trap types including fixed charge, traps and interface states. Image courtesy SEMATECH.

- MBE growth of $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ substrate
- HCl and $(NH_4)_2S$ surface cleaning
- ***In-situ*** **PH_3-passivation**
- MOCVD high-k deposition and *in-situ* PDA
- Sputter TaN deposition 150nm
- Lithography
- Gate etch and high-k etching
- Si implantation (50KeV/$1x10^{14}cm^{-2}$)
- ***S/D activation @ RTA 600ºC 60s, 700ºC 10s, 750ºC 5s***
- S/D and backside contacts
- Metal alloy annealing @ RTA 400ºC 60s

Figure 8. Process flow of self-aligned InGaAs channel MOSFET with plasma-PH_3 passivation process developed by Singapore researchers.

Zicronia

The SEMATECH research consortium has been working with a number of universities on zirconium dioxide (ZrO_2) as a gate dielectric for InGaAs channels. The universities are UTexas-Austin, SUNY-Albany, Oklahoma and Texas State [8].

The SEMATECH research has found that putting an interlayer of amorphous lanthanum aluminum oxide $(La)AlO_x$ before the ZrO_2 (Figure 6) can reduce the densities of various imperfections (Figure 7, Table 1) such as border traps (3x), effective fixed charges (1.5x) and interface traps (1.5x). The net effect of using this gate stack is a 50% improvement in drain current (I_d) and a 75% increase in transconductance (G_m). ALD was used to deposit the dielectric layers, producing MOS capacitors and long-channel nMOSFETs.

Although much work has been carried out on InGaAs using Al_2O_3 as dielectric, the researchers note that this material has a relatively low dielectric constant (7–9) for the needs of logic devices below 16nm. The dielectric constants of $LaAlO_2$ and ZrO_2 are higher: ~12 and ~32, respectively.

The reliability of the stacks was evaluated using positive- and negative-bias temperature instability (P/NBTI) cycle stress measurements of the threshold voltage. Use of an Al_2O_3 interlayer was found to improve the stress performance over just ZrO_2, but a $LaAlO_2/ZrO_2$ stack was even better.

Phosphine passivation

Singapore researchers (National University and the institutes of Microelectronics and of Materials Research and Engineering) have been looking at phosphine (PH_3) passivation techniques for use before dielectric deposition on InGaAs channels [9]. Previously, it had been a kind of mystery why such a treatment leads to improvement, since one might expect a disturbance of doping levels in the semiconductor layers.

However, the team has found from AFM and XPS measurements that what is achieved is a phosphorous nitride layer, rather than a replacement of arsenic atoms in the channel. The technique was then used to create high electron mobility in a metal gate/high-k dielectric inversion-mode InGaAs NMOSFET fabricated by a self-aligned gate-first scheme (Figure 8).

The InGaAs materials (53% In and 70% In) were grown on InP substrates using MBE. For the passivation and dielectric deposition, an ultra-high-vacuum (UHV) multi-chamber CVD system was used. This enabled a sequence of steps to be carried out without breaking the vacuum (including a post deposition anneal). The plasma passivation consisted of 1% PH_3 in nitrogen (Table 2). MOCVD was carried out to give layers of HfO_2 from $Hf(OC(CH_3)_3)_4$ precursor in oxygen, or hafnium aluminate (HfAlO) from $HfAl(MMP)_2(OiPr)_5$.

Table 2. Process conditions of one-minute plasma-PH_3 passivation by Singapore researchers.

Sample no.	Temp (ºC)	Plasma power (W)	Pressure (Torr)
A	430	200	0.7
B	430	200	0.3
C	550	No plasma	10
None		No treatment	

One passivation regime (sample B in Table 2) gave a 3x increase in drain current for HfO_2 dielectric and 10x for HfAlO over samples where AFM and XPS results reveal that a P_xN_y layer does not form (samples A and C). Thermal stability of the process under rapid thermal annealing

up to 750ºC was confirmed for enabling S/D activation, as used in self-aligned MOSFET production. In fact, higher-temperature annealing with HfO_2 dielectric leads to lower equivalent oxide thickness (EOT) values, possibly due to a densification effect. Gate leakage is also much reduced (Figure 9).

Characterization of a 600nm (0.6μm) gate nMOSFET with HfAlO dielectric showed a peak mobility of 2557cm²/V-s at an effective electric field of 0.24MV/cm. The maximum transconductance at 1V drain voltage was 378mS/mm. A drive current of 851mA/mm was measured with a gate bias of 3V and a drain voltage of 2V.

SEMATECH research has found that putting an interlayer of amorphous (La)AlO_x before the ZrO_2 can reduce the densities of various imperfections such as border traps (3x), effective fixed charges (1.5x) and interface traps (1.5x)

Although HfAlO results for thermal stability of EOT and HfO_2 nMOSFET characterizations are not reported in the IEDM paper, Dr Lee Sungjoo (S.J. Lee), one of the leaders of the work, reports that similar results have been obtained in these cases. ■

Mike Cooke is a freelance technology journalist who has worked in the semiconductor & advanced technology sectors since 1997.

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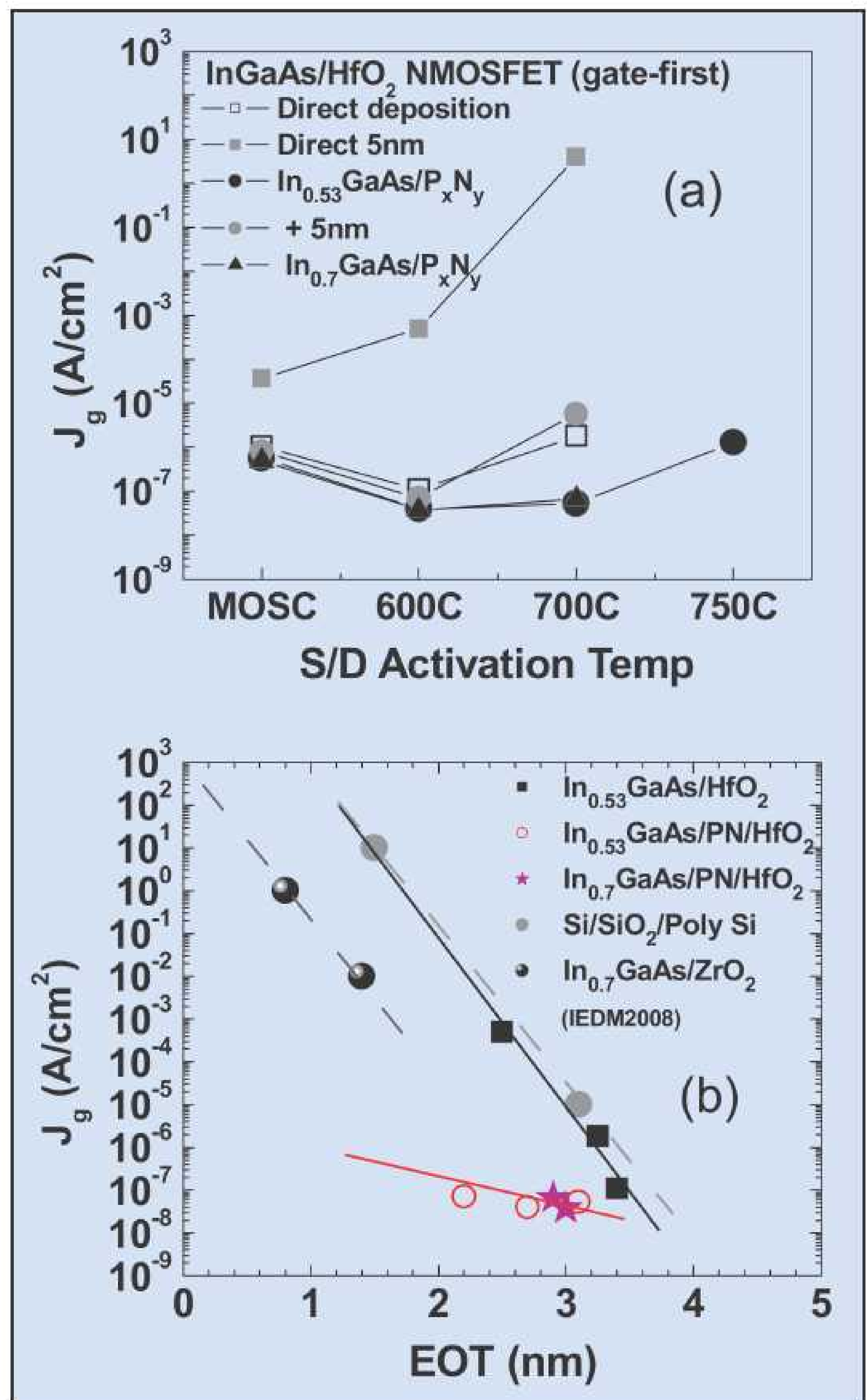

Figure 9. (a) Gate leakage current density (J_g) for Singapore HfO_2/InGaAs MOS capacitors vs S/D activation temperature and (b) comparison with reported results.

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